I CLAIM:

1. A method of controlling threshold voltage characteristics of a floating-gate field-effect transistor ("FET") in which a pair of source/drain regions are separated from each other by a channel portion of a body region that forms a pn junction with each source/drain region, a floating-gate electrode overlies the channel portion, and a control-gate electrode overlies the floating-gate electrode above the channel portion, the FET being in a first condition when its programmable threshold voltage is (a) less than a first transition value V_{T1} if the FET is of n-channel type and (b) greater than $-V_{T1}$ if the FET is of p-channel type, the FET being in a second condition when its programmable threshold voltage is (a) greater than a second transition value V_{T2} if the FET is of n-channel type and (b) less than $-V_{T2}$ if the FET is of p-channel type where V_{T2} exceeds or equals V_{T1}, a first body voltage at a body node being converted into a second body voltage applied to the body region, a first control voltage at a control node being converted into a second control voltage applied to the control-gate electrode, the method comprising:

placing the first body and first control voltages at respective body and control conditioning values different from each other such that the second body and second control voltages cause the FET to be in the first condition with its programmable threshold voltage (a) less than if the FET is of n-channel type or (b) greater than $-V_{T1}$ if the FET is of p-channel type regardless of whether the FET was immediately previously in the first or second condition; and

subsequently discharging the first body and first control voltages to respective body and control discharge values between the conditioning values, the body and control nodes being electrically connected to each other at least as the discharging act starts such that the first body and first control voltages begin to discharge largely simultaneously.

2. A method as in Claim 1 wherein the FET is a memory element that operates between a pair of supply voltages during reading of the memory element, one of the conditioning values being greater than both supply voltages, the other of the conditioning values being less than both supply voltages.

3. A method as in Claim 1 wherein V_{T2} exceeds V_{T1}.

4. A method as in Claim 1 wherein, for a specified voltage difference between the control-gate electrode and a specified one of the source/drain regions, an inversion layer (a)

occurs in the channel portion below the floating-gate electrode when the FET is in the first condition and (b) does not occur there when the FET is in the second condition.

5. A method as in Claim 1 wherein electrically insulating material separates the electrodes from each other and from a semiconductor body that contains the source/drain and body regions.

6. A method as in Claim 1 wherein the floating-gate electrode extends partially over both source/drain regions.

7. A method as in Claim 1 wherein the floating-gate electrode extends partially over only one of the source/drain regions, the control-gate electrode extending partially over the other of the source/drain regions.

8. A method as in Claim 1 wherein the floating-gate electrode extends partially over only one of the source/drain regions, a select-gate electrode overlying the channel portion and extending partially over the other of the source/drain regions.

9. A method as in Claim 8 wherein electrically insulating material separates the electrodes from each other and from a semiconductor body that contains the source/drain and body regions.

10. A method as in Claim 1 wherein the body and control nodes are physically connected to each other through a switch, the discharging act including closing the switch to electrically connect the body and control nodes to each other.

11. A method as in Claim 10 wherein the body and control nodes are also physically connected to each other through a resistor.

12. A method as in Claim 1 wherein the discharging act includes, subsequent to its start, performing at least one of:

electrically connecting the body node to a source of a body reference voltage approximately equal to the body discharge value; and

electrically connecting the control node to a source of a control reference voltage approximately equal to the control discharge value.

13. A method as in Claim 12 wherein both of the electrically connecting acts are performed.

14. A method as in Claim 13 wherein the electrically connecting acts are initiated in response to one of the first body and first control voltages reaching a specified value.

15. A method as in Claim 13 wherein the electrical connecting acts are initiated in response to the first control voltage reaching a specified intermediate control value between the control conditioning value and the control discharge value.

16. A method as in Claim 1 wherein the control discharge value is closer to the control conditioning value than is the body discharge value while the body discharge value is closer to the body conditioning value than is the control discharge value.

17. A method as in Claim 1 wherein the FET is of n-channel type.

18. A method as in Claim 17 wherein:

the body conditioning value exceeds the control conditioning value;

the placing act comprises (i) increasing the first body voltage to cause the second body voltage to increase and (ii) decreasing the first control voltage to cause the second control voltage to decrease; and

the discharging act comprises (i) decreasing the first body voltage to cause the second body voltage to decrease and (b) increasing the first control voltage to cause the second control voltage to increase.

19. A method of controlling threshold-voltage characteristics of a group of like-polarity floating-gate field-effect transistors ("FETs") of an electrically erasable programmable read-only memory where each FET has a pair of source/drain regions separated from each other by a channel portion of a body region that forms a pn junction with each source/drain region, a floating-gate electrode overlies the channel portion, and a control-gate electrode overlies the floating-gate electrode above the channel portion, each FET being in an erased condition when its programmable threshold voltage is less than a first transition value V_{T1} if that FET is of n-channel type and (b) greater than $-V_{T1}$ if that FET is of p-channel type, each FET being in a programmed condition when its programmable threshold voltage is (a) greater than a second transition value V_{T2} if that FET is of n-channel type and (b) less than $-V_{T2}$ if the FET is of p-channel type where V_{T2} exceeds or equals V_{T1}, a first body voltage at a body node being converted into a second body voltage applied to the body region, a first control voltage at a

control node being converted into a plurality of second control voltages each applied to at least one of the control-gate electrodes, the method comprising:

placing the first body and first control voltages at respective body and control conditioning values different from each other such that the second body and second control voltages cause each FET to be in its erased condition with its programmable threshold voltage (a) less V_{T1} if that FET is of n-channel type or (b) greater than $-V_{T1}$ if that FET is of p-channel type regardless of whether that FET was immediately previously in its erased or programmed condition; and

subsequently discharging the first body and first control voltages to respective body and control discharge values between the conditioning values, the body and control nodes being electrically connected to each other at least as the discharging act starts such that the first body and first control voltages begin to discharge largely simultaneously.

20. A method as in Claim 19 wherein the FET is a memory element that operates between a pair of supply voltages during reading of the memory element, one of the conditioning values being greater than both supply voltages, the other of the conditioning values being less than both supply voltages.

21. A method as in Claim 19 wherein each FET, if any, not in its erased condition immediately previous to the placing act enters its erased condition during the placing act substantially simultaneously as each other FET, if any, not in its erased condition immediately previous to the placing act.

22. A method as in Claim 19 further including placing at least one of the FETs in its programmed condition while at least one other of the FETs remains in its erased condition.

23. A method as in Claim 19 further including providing a specified voltage difference between the control-gate electrode of each FET and a specified one of its source/drain regions such that an inversion layer (a) occurs in the channel portion of that FET below its floating-gate electrode when that FET is in its erased condition and (b) does not occur there when that FET is in its programmed condition.

24. A method as in Claim 19 wherein the discharging act includes, subsequent to its start, performing at least one of:

electrically connecting the body node to a source of a body reference voltage approximately equal to the body discharge value; and

electrically connecting the control node to a source of a control reference voltage approximately equal to the control discharge value.

25. A method as in Claim 24 wherein both of the electrically connecting acts are performed.

26. A method as in Claim 25 wherein the electrically connecting acts are initiated in response to one of the first body and first control voltages reaching a specified value.

27. A electronic circuit comprising:

a floating-gate field-effect transistor ("FET") in which a pair of source/drain regions are separated from each other by a channel portion of a body region that forms a pn junction with each source/drain region, a floating-gate electrode overlies the channel portion, and a control-gate electrode overlies the floating-gate electrode above the channel portion, the FET being in a first condition when its programmable threshold voltage is (a) less than a first transition value V_{T1} if the FET is of n-channel type and (b) greater than $-V_{T1}$ if the FET is of p-channel type, the FET being in a second condition when its programmable threshold voltage is (a) greater than a second transition value V_{T2} if the FET is of n-channel type and (b) less than $-V_{T2}$ if the FET is of p-channel type where V_{T2} exceeds or equals V_{T1}, a first body voltage at a body node being converted into a second body voltage applied to the body region, a first control voltage at a control node being converted into a second control voltage applied to the control-gate electrode;

conditioning circuitry for selectively placing the first body and first control voltages at respective body and control conditioning values different from each other such that the second body and second control voltages cause the FET to be in the first condition with its programmable threshold voltage (a) less than V_{T1} if the FET is of n-channel type or (b) greater than $-V_{T1}$ if the FET is of p-channel type regardless of whether the FET was immediately previously in the first or second condition; and

voltage discharge circuitry for discharging the first body and first control voltages to respective body and control discharge values between the conditioning values, the voltage discharge circuitry comprising common discharge circuitry for electrically connecting the body and control nodes to each other at least as the first body and first control voltages start discharging such that they begin to discharge largely simultaneously.

28. A circuit as in Claim 31 wherein the FET is a memory element that operates between a pair of supply voltages during reading of the memory element, one of the conditioning values being greater than both supply voltages, the other of the conditioning values being less than both supply voltages.

29. A circuit as in Claim 27 wherein V_{T2} exceeds V_{T1}.

30. A circuit as in Claim 27 further including accessing circuitry for selectively supplying a specified voltage difference between the control-gate electrode and a specified one of the source/drain regions such that an inversion layer (a) occurs in the channel portion below the floating-gate electrode when the FET is in the first condition and (b) does not occur there when the FET is in the second condition.

31. A circuit as in Claim 27 wherein electrically insulating material separates the electrodes from each other and from a semiconductor body that contains the source/drain and body regions.

32. A circuit as in Claim 27 wherein the floating-gate electrode extends partially over both source/drain regions.

33. A circuit as in Claim 27 wherein the floating-gate electrode extends partially over only one of the source/drain regions, the control-gate electrode extending partially over the other of the source/drain regions.

34. A circuit as in Claim 27 wherein the floating-gate electrode extends partially over only one of the source/drain regions, a select-gate electrode overlying the channel portion and extending partially over the other of the source/drain regions.

35. A circuit as in Claim 34 wherein electrically insulating material separates the electrodes from each other and from a semiconductor body that contains the source/drain and body regions.

36. A circuit as in Claim 27 wherein the common discharge circuitry includes a switch through which the body and control nodes are physically connected to each other, the switch being closed as the first body and first control voltages discharge so as to electrically connect the body and control nodes to each other.

37. A circuit as in Claim 36 wherein the common discharge circuitry includes a resistor through which the body and control nodes are physically connected to each other.

38. A circuit as in Claim 37 wherein the voltage discharge circuitry further includes at least one of:

body-line discharge circuitry for electrically connecting the body node to a source of a body reference voltage approximately equal to the body discharge value; and

control-line discharge circuitry for electrically connecting the control node to a source of a control reference voltage approximately equal to the control discharge value.

39. A circuit as in Claim 38 wherein both the body-line discharge circuitry and the control-line discharge circuitry are present in the voltage discharge circuitry.

40. A circuit as in Claim 39 wherein the body-line and control-line discharge circuitries respectively initiate discharge of the first body and first control voltages in response to one of them reaching a specified value.

41. A circuit as in Claim 39 wherein the body-line and control-line discharge circuitries respectively initiate discharging of the first body and first control voltages in response to the first control voltage reaching a specified value.

42. A circuit as in Claim 27 wherein the control discharge value is closer to the control conditioning value than is the body discharge value while the body discharge value is closer to the body conditioning value than is the control discharge value.

43. An electrically erasable programmable read-only memory ("EPROM") comprising:

a group of memory elements respectively comprising like-polarity floating-gate field-effect transistors ("FETs") wherein each FET has a pair of source/drain regions separated from each other by a channel portion of a body region that forms a pn junction with each source/drain region, a floating-gate electrode overlies the channel portion, and a control-gate electrode overlies the floating-gate electrode above the channel portion, the FET being in a erased condition when its programmable threshold voltage is (a) less than a first transition value V_{T1} if that FET is of n-channel type and (b) greater than $-V_{T1}$ if that FET is of p-channel type, each FET being in a programmed condition when its programmable threshold voltage is (a) greater than a second transition value V_{T2} if that FET is of n-channel type and (b) less than $-V_{T2}$

if that FET is of p-channel type where V_{T2} exceeds or equals V_{T1}, a first body voltage at a body node being converted into a second body voltage applied to the body region, a first control voltage at a control node being converted into a plurality of second control voltages each applied to at least one of the control-gate electrodes;

conditioning circuitry for selectively placing the first body and first control voltages at respective body and control conditioning values different from each other such that the second body and second control voltages cause each FET to be in the erased condition with its programmable threshold voltage (a) less than V_{T1} if that FET is of n-channel type or (b) greater than $-V_{T1}$ if that FET is of p-channel type regardless of whether that FET was immediately previously in the erased or programmed condition; and

voltage discharge circuitry for discharging the first body and first control voltages to respective body and control discharge values between the conditioning values, the voltage discharge circuitry comprising common discharge circuitry for electrically connecting the body and control nodes to each other at least as the first body and first control voltages start discharging such that they begin to discharge largely simultaneously.

44. An EPROM as in Claim 43 wherein the memory elements operate between a pair of supply voltages during reading of the memory elements, one of the conditioning values being greater than both supply voltages, the other of the conditioning values being less than both supply voltages.

45. An EPROM as in Claim 43 wherein, when the first body and first control voltages are placed at their respective body and control values, the conditioning circuitry causes each FET, if any, not immediately previously in its erased condition to enter its erased condition substantially simultaneously as each other FET, if any, not immediately previously in its erased condition.

46. An EPROM as in Claim 45 further including programming circuitry for selectively placing the FETs in their programmed conditions.

47. An EPROM as in Claim 43 wherein at least one of the FETs is in its programmed condition when at least one other of the FETs is in its erased condition.

48. An EPROM as in Claim 43 wherein the voltage discharge circuitry further includes at least one of:

body-line discharge circuitry for electrically connecting the body node to a source of a body reference voltage approximately equal to the body discharge value; and

control-line discharge circuitry for electrically connecting the control node to a source of a control reference voltage approximately equal to the control discharge value.

49. An EPROM as in Claim 48 wherein both the body-line discharge circuitry and the control-line discharge circuitry are present in the voltage discharge circuitry.

50. An EPROM as in Claim 49 wherein the body-line and control-line discharge circuitries respectively initiate discharge of the first body and first control voltages in response to one of them reaching a specified value.